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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/161,405	09/28/1998	HIRAKU KOZUKA	862.2480	7603

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EXAMINER
WHIPKEY, JASON T

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/161,405	Applicant(s) KOZUKA, HIRAKU
	Examiner Jason T. Whipkey	Art Unit 2612

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8,11,14 and 33-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,11,14,33-35,37 and 38* is/are rejected.

7)☒ Claim(s) *36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 2, 2003 has been entered.

Drawings

2. The corrected drawings were received on June 2, 2003. These drawings are approved.

Response to Arguments

3. Applicant's arguments with respect to claims 33 and 38 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 33-35, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent No. 5,321,528) in view of Kondou (U.S. Patent No. 5,021,888) and further in view of Ansari (U.S. Patent No. 6,288,742).

Regarding claims 33 and 38, Nakamura discloses an image sensor consisting of multiple sensor chips that are "aligned" (column 2, line 66, through column 3, line 4), indicating they are mounted on a base. Each chip — 1-1 in Figure 1, for example — has an output bus (unlabeled) connecting the drains of transistors 6-1-1, 6-1-2, etc., which are connected to photoconversion cells 2-1-1, 2-1-2, etc. The output bus in each chip is used to output light signal voltage V2 (column 3, lines 52-55) and noise signal voltage V1 (column 3, lines 36-41). Amplifiers 9-1 *et al.* output the signal from the output bus of each chip.

An amplifier circuit, consisting of parts 33-39 shown in Figure 3, receives the output of an inter-chip bus. Buffer amplifier 33 receives the both the noise signal V1 (column 4, lines 3-8) and the light signal V2 (column 4, lines 16-20) from the bus. Capacitor 35 receives these signals and finds the difference (column 4, lines 16-30). Components 33-39 comprise a correction circuit 140 (column 5, lines 11-16), and correction circuit 140 is part of a printed circuit board (column 5, lines 56-58).

Nakamura is silent with regard to including a noise reduction circuit on the base with the sensor chips.

Kondou discloses an imaging device (Figure 1) where flexible printed circuit board 11 is attached to solid state imaging element 10 (column 3, lines 29-31). Included on flexible printed circuit board 11 is a plurality of components 13, including a noise reduction circuit (column 3, lines 32-35).

An advantage to including a noise reduction circuit on a printed circuit board with an imaging device is that a strong, dependable, permanent connection can be made between the imager and the noise reduction circuit, which makes the chance of noise resulting from a poor connection less likely. For this reason, it would have been obvious at the time of invention to have Nakamura include his noise-reducing buffer amplifier on the same board as the image sensor.

Nakamura and Kondou are silent with regard to using one noise reduction circuit to process signals from a plurality of image sensing devices.

Ansari discloses a video camera with multiple image sensors. Figure 2C shows that a common correlated double sampling circuit 6 can be used to process signals from each of the two CCDs 5 (column 3, line 66, through column 4, line 15).

As stated in column 3, lines 63-66, an advantage to using one CDS circuit is that the cost of the system can be reduced. For this reason, it would have been obvious at the time of invention to have Nakamura's and Kondou's system use a single noise-correction circuit with a plurality of image sensors.

Nakamura is also silent with regard to including an output terminal connected to the output of the noise-reducing buffer amplifier.

Kondou shows in Figure 1 that connection pads 15 have extension cables 16 connected to them, wherein connection pads 15 are also connected to the output of components 13 (column 3, lines 35-37).

An advantage to including output terminals on a mounting board is that a connection may be made to a card slot or wiring at a location that requires the least disturbance of the components on the board. This prevents components from being damaged. For this reason, it would have been obvious at the time of invention to have Nakamura include output connections on the outside of his mounting board.

Regarding claim 34, Nakamura discloses a differential circuit (capacitor 35) as described above. Additionally, capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

Regarding claim 35, the chip is reset via reset terminal 24 (column 3, lines 39-40). After the inter-chip bus is reset, clamping circuit 35-38 clamps the reset state (column 4, lines 5-12).

Regarding claim 37, Nakamura shows that capacitor 35 is part of a clamping circuit consisting of parts 35-38. The clamping circuit clamps the signal using clamping voltage VC from clamped voltage source 38 (column 4, lines 11-12).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari and Surisawa (U.S. Patent No. 6,215,521).

Claim 8 may be treated like claim 33. However, Nakamura is silent with regard to using a power supply voltage with the photosensor chips that is lower than the power supply voltage supplied to the processing means.

Surisawa discloses an image sensor on a substrate 1 (Figure 10A). The voltage V_{sub} supplied to the substrate is larger than the voltage V_D supplied to the image sensor (column 13, lines 6-8). The advantage to having separate power supplies is that the appropriate voltage may be supplied to each component without excess, which saves power. For this reason, it would have been obvious to have separate power supplies for the chips and the substrate.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari and Hamasaki.

Claim 11 may be treated like claim 33. However, Nakamura is silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would

have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Kondou and further in view of Ansari, Surisawa, and Hamasaki.

Claim 14 may be treated like claim 8. However, Nakamura is silent with regard to isolating the ground wiring for the photosensor chips and the processing circuitry.

Hamasaki discloses an image pickup device on a substrate 72 (Figure 4). Output section 78 is also included on substrate 72. Grounding wiring 80 grounds the imaging area (column 6, lines 33-42). Grounding wiring 88 grounds output section 78 (column 6, lines 51-56). As stated in column 6, line 68, through column 7, line 7, this prevents output section 78 from affecting the sensing section. For this reason, it would have been obvious for Nakamura's system to include separate ground wiring for the photosensor chips and the processing circuitry.

Allowable Subject Matter

9. Claim 36 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art could be located that teaches or fairly suggests a noise compensation circuit with a plurality of serially connected clamp circuits connected to the output of an image sensor.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819. The examiner can normally be reached Monday through Friday from 9 A.M. to 6:30 P.M. eastern daylight time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communication and (703) 872-9315 for After Final communication.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

Response to this action should be mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to the appropriate number above for communications intended for entry. (For informal or draft communications, please label "**PROPOSED**" or "**DRAFT**".)

Hand-delivered responses should be brought to the sixth floor receptionist of Crystal Park II, 2121 Crystal Drive in Arlington, Virginia.

JTW
JTW
July 14, 2003

NGOC-YEN VU
PRIMARY EXAMINER